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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,056	03/30/2004	Masahiro Ito	Q80548	1303

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EXAMINER	
SITTA, GRANT	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/812,056	ITO ET AL.	
	Examiner	Art Unit	
	Grant D. Sitta	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/8/2006,5/04/2006/,3/30/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3 and 5-8 rejected under 35 U.S.C. 102(e) as being anticipated by Shigeta et al (US 6,646,625) hereinafter Shigeta.

3. In regards to claim 1, Shigeta discloses a bit rate converter (fig. 15, (331)) for converting an M-bit input video signal (fig. 2 (D)) to an N-bit output video (fig. 2 (HD)) signal by retaining gray levels (fig. 15 "display data") of the M-bit input video signal (fig. 2 (D)), wherein N is smaller than M (col. 12, lines 15-50); and a gamma correction memory (fig. 2 (4)) in which a plurality of N-bit input gray levels are mapped to a plurality of output gray levels (fig. 20) which are distributed on a non-linear curve (fig. 20) complementary to a non-linear curve on which gray levels of a display device are distributed (fig. 20, col. 16, lines 12-70), said memory delivering one of the output gray

levels when said N-bit output video signal of said bit rate converter corresponds to one of the N-bit input gray levels (fig. 20, col 16, lines 12-70).

4. In regards to claim 2, Shigeta discloses where gray levels are represented by N bits (col. 6 lines 23-26).

5. In regards to claim 3, Shigeta discloses wherein said output gray scale values are interpolated gray levels of the input gray levels (col. 6 18-34).

6. In regards to claim 5, Shigeta discloses wherein said bit rate converter comprises means for truncating lower significant bits of the M-bit video signal, representing the truncated lower significant bits by a different number of binary-1's, and distributing the binary-1's over a varying number of subsequent frames depending on the truncated lower significant bits (col. 25, lines 25-50).

7. In regards to claim 6, Shigeta discloses wherein said bit rate converter comprises: a first adder (fig. 15. (342)) for summing a binary-1 to the least significant bit position of higher N bits of the M-bit input video signal (fig. 15 "2 bits"); a first multiplexer for selecting an output of said first adder (fig. 15 (335)) or said higher N bits in response

to a first control signal (fig. 15 signal from 334); a first frame memory (fig. 15 (336) delay circuit) for storing an output of said first multiplexer; a second adder for summing a binary-1 to an output of the first frame memory; (fig. 15 (335)) a second multiplexer (fig. 15 (339)) for selecting an output of said second adder (fig. 15 (332)) or an output of said first frame memory (fig. 15 (336) delay circuit) in response to a second control signal; a second frame memory (fig. 15 (334) delay circuit) for storing an output of said second multiplexer (fig. 15 (339)); a third adder (fig. 15 (333)) for summing a binary-1 to an output of the second frame memory (fig. 15 (334) delay circuit); a third multiplexer (fig. 15 (341)) for selecting an output of said third adder (fig. 15 (333)) or an output of said second frame memory (fig. 15 (334) delay circuit) in response to a third control signal; a third frame memory (fig. 15 (338)) for storing an output of said third multiplexer(fig. 15 (341)); and control means for producing said first control signal only, said first and second control signals simultaneously, or said first, second and third control signals simultaneously, depending on the truncated lower significant bits (fig. 15 "2 bits"). (col. 12 lines 20-70).

8. In regards to claim 7, Shigeta discloses wherein said bit rate converter comprises means for truncating lower significant bits of the M-bit video signal so that N bits are left in the input video signal, and dithering the N bits according to the truncated lower significant bits (col. 13, lines 35-45).

9. In regards to claim 8, Shigeta discloses wherein said bit rate converter comprises: an adder for summing a binary-1 (fig 15 (333)) to higher N bits of the M-bit input video signal; a multiplexer (fig 15 (335)) for selecting an output of said adder or said higher N bits of the M-bit input video signal in response to a control signal; and a comparator for producing said control signal by making a comparison between lower significant bits of said M-bit input video signal and a threshold value (fig 15, The comparator is the circuit as a whole col. 13, lines 1-15).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shigeta in view of Lee et al. (US 7,030,846) hereinafter, Lee.

4. In regards to claim 4, Shigeta discloses the limitations of claim 1,

Shigeta differs from the claimed invention in that Shigeta does not disclose wherein said output gray scale values are represented by M bits.

However, Lee teaches a system and method where gray scale output values are represented by M bits (Fig 8 (110) col. 7-8, lines 55-10 of Lee).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Shigeta to include the use of output gray scale values that are represented by M bits as taught by Lee in order to allow adaptive color correction while securing constant color sensation as stated in (col. 2, lines 50-55 of Lee).

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Grant D. Sitta whose telephone number is 571-270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-270-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Grant D. Sitta

May 22, 2007

XIAO WU
SUPERVISORY PATENT EXAMINER